

Nixon Peabody LLP

Attorneys at Law

Suite 900

401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000

Fax: (202) 585-8080

PRIVILEGE AND CONFIDENTIALITY NOTICE
 The information in this fax is intended for the named recipients only. It contains privileged and confidential matter. If you have received this fax in error, please notify us immediately by a collect telephone call to (202) 585-8000 and return the original to the sender by mail. We will reimburse you for postage. Do not disclose the contents to anyone. Thank you.

FAX**RECEIVED**
CENTRAL FAX CENTER**OCT 13 2005****Date:** October 13, 2005**Pages (including cover):** 5**To:** Issue/Publication Fee Branch**Fax:** 571-273-2885**Ph:****From:** Donald R. Studebaker, Reg. No. 32,815**Docket No.** 031794-13**Message:** The following documents are being presented for facsimile filing in the United States Patent and Trademark Office:

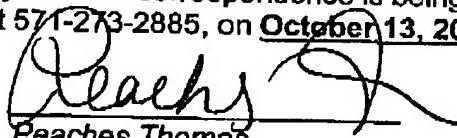
1. Amendment Pursuant to 37 C.F.R. §1.312
2. Notice of Allowance and Issue Fee Transmittal – Part B (PTOL-85)
3. Permission to charge the Deposit Account No. 19-2380 in the amount of \$1730.00 representing \$1400.00 for Issue Fee, \$300.00 Publication Fee and \$30.00 for Advance Order of 10 Patent Copies.

In re Patent Application of
 Inventor(s): Yoshimasa SEKINO
 Application No. 10/811,836
 Filed: March 30, 2004
 For: POWER-ON RESET CIRCUIT

Due Date: **October 13, 2005**
 Docket Number: 031794-13Date: **October 13, 2005**
 DRS/pt**CERTIFICATE OF FACSIMILE TRANSMISSION [37 CFR 1.8(a)]**

I hereby certify that this correspondence is being facsimile transmitted to the USPTO at 571-273-2885, on October 13, 2005.

Signature:
 Name:



Peaches Thomas

RECEIVED
OIPE/AP**OCT 17 2005**

Nixon Peabody LLP
Attorneys at Law

Suite 900
401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000

Fax: (202) 585-8080

PRIVILEGE AND CONFIDENTIALITY NOTICE
The information in this fax is intended for the named recipients only. It contains privileged and confidential matter. If you have received this fax in error, please notify us immediately by a collect telephone call to (202) 585-8000 and return the original to the sender by mail. We will reimburse you for postage. Do not disclose the contents to anyone. Thank you.

FAX**RECEIVED**
CENTRAL FAX CENTER

OCT 13 2005

Date: October 13, 2005 **Pages (including cover):** 5
To: Issue/Publication Fee Branch **Fax:** 571-273-2885 **Ph:**
From: Donald R. Studebaker, Reg. No. 32,815 **Docket No.** 031794-13
Message: The following documents are being presented for facsimile filing in the United States Patent and Trademark Office:

1. Amendment Pursuant to 37 C.F.R. §1.312
2. Notice of Allowance and Issue Fee Transmittal – Part B (PTOL-85)
3. Permission to charge the Deposit Account No. 19-2380 in the amount of \$1730.00 representing \$1400.00 for Issue Fee, \$300.00 Publication Fee and \$30.00 for Advance Order of 10 Patent Copies.

In re Patent Application of
Inventor(s): Yoshimasa SEKINO
Application No. 10/811,836
Filed: March 30, 2004
For: POWER-ON RESET CIRCUIT

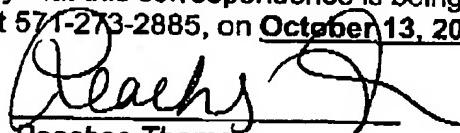
Due Date: October 13, 2005
Docket Number: 031794-13

Date: October 13, 2005
DRS/pt

CERTIFICATE OF FACSIMILE TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being facsimile transmitted to the USPTO at 571-273-2885, on October 13, 2005.

Signature:
Name:



Peaches Thomas

Docket No. 031794-13
Serial No. 10/811,836
Page 1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
CENTRAL FAX CENTER

In re Patent Application of:

Yoshimasa SEKINO

Serial No. 10/811,836

Filed: 3/30/2004

For: POWER-ON RESET CIRCUIT

)

) Group Art Unit: 2816

) Examiner: Terry D. Cunningham

) Confirmation: 3050

) October 13, 2005

OCT 13 2005

AMENDMENT PURSUANT TO 37 C.F.R. §1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to issuance, please amend the above identified application as follows:

IN THE CLAIMS:

Please amend claim 3 as follows.

3. (Currently Amending) A power-on reset circuit comprising:

a first capacitor connected between a power supply line and a first node;

a first MOS transistor connected between said first node and a second node, and

ON/OFF controlled based on a first pulse signal;

a second MOS transistor connected between said second node and a reference

potential, and ON/OFF controlled based on a second pulse signal;

a second capacitor connected between said second node and said reference potential;

a timing control unit for generating said first and second pulse signals in synchronism with a clock signal externally applied thereto; and

an output portion outputting a reset signal when the potential of said internal node an

BEST AVAILABLE COPY